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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,974	10/18/2004	Brent A. Anderson	BUR920040083US1	5973

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EXAMINER	
FORDE, REMMON R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,974	ANDERSON ET AL.	
	Examiner	Art Unit	
	Remmon R. Fordé	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response To Election

The Examiner hereby acknowledges Applicant's election of claims 1-11, without traverse, in correspondence filed 02/04/2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-7 and 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugii et al..

Regarding claims 1, 2, 6 and 7, referencing Figure 49, Sugii et al. discloses a device structure provided with a SOI wafer provided with a substrate (1); a buried isolation layer (13) over the substrate; a semiconductor layer (5) over the buried isolation layer (13); a fin field effect transistor (FinFet) over the buried isolation layer (13); and a field effect transistor (FET) in the substrate (1), wherein a gate region (8) of the FET is planar to a gate region of the FinFet (8). (Paragraph [0169] and [0182].)

Regarding claims 4 and 9, referencing Figure 49, Sugii et al. further discloses providing for the FET: FET source/drain regions (12) on opposite sides of the FET gate region (8); and a gate dielectric layer (7) between the FET gate region (8) and the substrate (1). (Paragraph [0182].)

Regarding claims 5 and 11, referencing Figures 41 and 49, Sugii et al. further discloses a shallow trench isolation region (6) in the substrate (1). (Paragraph [0167] and [0182].)

Regarding claim 10, referencing Figures 49, Sugii et al. further discloses that the buried isolation layer is buried oxide. (Paragraph [0182].)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugii et al. in view of Wu et al..

Referencing Figure 49, Sugii et al. discloses a device structure provided with a SOI wafer provided with a substrate (1); a buried isolation layer (13) over the substrate; a semiconductor layer (5) over the buried isolation layer (13); a fin field effect transistor (FinFet) over the buried isolation layer (13); and a field effect transistor (FET) in the

substrate (1), wherein a gate region (8) of the FET is planar to a gate region of the FinFet (8). (Paragraph [0169] and [0182].)

Unfortunately, Sugii et al. fails to disclose the specific claim limitations of the FinFet device (i.e. Sugii et al. discloses a FinFet device but fails to show the actual structure.

However, referencing Figures 1-11A, Wu et al. discloses a FinFet CMOS device structure provided with a semiconductor layer (3) comprising sidewalls; a first dielectric layer (4) over the semiconductor layer; a second dielectric layer (7) along each of the sidewalls of the semiconductor layer; the FinFet gate region (8) over the first and second dielectric layers; and FinFet source/drain regions (30/40) on opposite sides of the FinFet gate region (8). Wu et al. further teaches that the ability to fabricate a FinFet type device entirely in a SOI layer has allowed miniaturization of device features to be successfully accomplished with less risk of the yield degrading phenomena such as short channel effects when compared to counterpart devices formed in a semiconductor substrate. (Column 1, lines 27-35.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the disclosed FinFet structure of Wu et al. for the FinFet device as disclosed by Sugii et al. because the conventional FinFet structure is well known in the art and Wu et al. teaches that the ability to fabricate a FinFet type device entirely in a SOI layer has allowed miniaturization of device features to be successfully accomplished with less risk of the yield degrading phenomena such as

short channel effects when compared to counterpart devices formed in a semiconductor substrate. (Column 1, lines 27-35.)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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